**Studytonight – CAO test 7 – Aditya Jain**

1. **The digital information is stored on the hard disk by \_\_\_\_\_\_\_\_\_\_\_\_**a) **Applying a suitable electric pulse**b) Applying a suitable magnetic field  
   c) Applying a suitable nuclear field  
   d) By using optic waves
2. **The main reason for the discontinuation of semi-conductor based storage devices for providing large storage space is \_\_\_\_\_\_\_\_\_**a) Lack of sufficient resources  
   **b) High cost per bit value**c) Lack of speed of operation  
   d) None of the mentioned

Explanation: In case of semi-conductor based memory technology, we get speed but the increase in the integration of various devices the cost is high.

1. **One of the most widely used schemes of encoding used is \_\_\_\_\_\_\_\_\_**a) NRZ-polar  
   b) RZ-polar  
   c) **Manchester**  
   d) Block encoding

Explanation: The Manchester encoding used is also called as phase encoding and it is used to encode both clock and data.

1. **The logic operations are simpler to implement using logic circuits.**a) **True**b) False

Explanation: The logic circuits are made using the logical gates such as AND, OR, NOT, XOR, etc. and hence are easier to understand the design and implement them.

1. **A hard disk with 20 surfaces will have \_\_\_\_\_ heads.**a) 10  
   b) 5  
   c) 1  
   d) **20**

Explanation: Each surface will have its own head to perform read/write operation.

1. **The read/write heads must be near to disk surfaces for better storage.**a) **True**b) False

Explanation: By maintaining the heads near to the surface, greater bit densities can be achieved, thereby saving a great amount of memory.

1. **For the synchronization of the read head, we make use of a \_\_\_\_\_\_\_**a) Framing bit  
   b) Synchronization bit  
   c) **Clock**d) Dirty bit

Explanation: The clock makes it easy to distinguish between different values read by head.

1. **The logic operations are implemented using \_\_\_\_\_\_\_ circuits.**a) Bridge  
   b) Logical  
   **c) Combinatorial**d) Gate

Explanation: The combinatorial circuits are the circuits made using only the basic universal gates (AND, OR, NOT, etc.).

1. **The drawback of Manchester encoding is \_\_\_\_\_\_\_\_\_**a) The cost of the encoding scheme  
   b) The speed of encoding the data  
   c) The Latency offered  
   **d) The low bit storage density provided**

Explanation: The space required to represent each bit must be large enough to accommodate two changes in magnetization.

1. **A \_\_\_\_\_\_\_ gate is used to detect the occurrence of an overflow.**

a) NAND  
b) **XOR**c) XNOR  
d) AND

Explanation: The overflow is detected by cn^cn-1 (‘^’ indicates XOR operation).

1. **\_\_\_\_\_ pushes the heads away from the surface as they rotate at their standard rates.**a) Magnetic tension  
   b) Electric force  
   **c) Air pressure**d) None of the mentioned

Explanation: Due to the speed of rotation of the disc, air pressure develops in the hard disk.

1. **Which of the following is true in reference to the CARRY in the ripple adders.**a) Are generated at the beginning only  
   b) **Must travel through the configuration**c) Is generated at the end of each operation  
   d) None of the mentioned

Explanation: The carry must pass through the configuration of the circuit till it reaches the particular step.

1. **In a normal adder circuit the delay obtained in generation of the output is \_\_\_\_\_\_\_  
   a) 2n + 2**b) 2n  
   c) n + 2  
   d) None of the mentioned

Explanation: The 2n delay cause of the carry generation and the 2 delay due to the XOR operation.

1. **The air pressure can be countered by putting \_\_\_\_\_\_ in the head-disc surface arrangement.**a) Air filter  
   **b) Spring mechanism**c) coolant  
   d) None of the mentioned

Explanation: The spring mechanism pushes the head along the surface to reduce the air pressure effect.

1. **The usual implementation of the carry circuit involves \_\_\_\_\_\_\_\_\_**a) AND and OR gates  
   b) **XOR**c) NAND  
   d) XNOR

Explanation: Carry Circuit are involved in the implementation of Full and Half Adder.